Analog Communication Laboratory Manual

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This is a laboratory manual for analog communication experiments. It mostly adheres to the syllabus of the University of Calicut.

This project is hosted at: https://github.com/kavyamanohar/analogcommunication
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Preface

This laboratory manual has been prepared as a guideline to help students of undergraduate courses to carry out basic experiments in analog communication in the laboratory. This book is written in a way that a student with basic understanding on electronic circuit theory can learn the theory and experiment the basics of analog communication techniques.

Along with circuit components, introductions, an appendix section which discuss the data sheet details of that component is provided. Every experiment is explained with associated circuit diagrams, which were drawn using gEDA schemetic editor. Signal waveforms associated with the experiments were simulated in octave and given along with the experiment. Data, documents or diagrams used in the book which were taken from external sources are linked to the original sources as footnotes.

This is a work in progress version of the laboratory manual. Suggestions on improvement in conceptual clarity, diagrams, typography are most welcome. Share whatever you feel about the book- it is yours.

Kavya Manohar

Acknowledgements

Thank you for going through this work. Thanks in advance for your valuable feedbacks that would help improve this book.

Thanks a lot for the lectures and notes of Prof. Madhavan Nair, Retired Professor, College of Engineering Trivandrum, which helped me to draft this manual.

Thanks to my colleagues at Aryanet Institute of Technology for their encouragement and support. Special thanks to Sathyan P. for being with me experimenting in the laboratory. Thanks to my students who helped me improve the contents with timely comments.

Thanks to all free knowledge enthusiasts- especially to those who have created and shared electronics and communication engineering related contents to various public domain sources. Your efforts have helped a lot in the making of this book.

Thanks Santhosh, for what you are to me.

Kavya Manohar

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Chapter 1

Introduction to Analog Communication

[1]Communication is the transfer of information from one place to another. Radio communication uses electrical energy to transmit information.

The transmitted information is the **intelligence signal** or **message signal**. Message signals are in the **Audio Frequency (AF)** range of low frequencies from about 20 Hz to 20 kHz.

The **Radio Frequency (RF)** is the carrier signal. Carrier signals have high frequencies that range from 10 kHz up to about 1000 GHz. A radio transmitter sends the low frequency message signal at the higher carrier signal frequency by combining the message signal with the carrier signal.

Modulation is the process of changing a characteristic of the carrier signal with the message signal. In the transmitter, the message signal modulates the carrier signal. The modulated carrier signal is sent to the receiver where **demodulation** of the carrier occurs to recover the message signal.

IMPORTANT TERMS

- **Electromagnetic waves** - the radiant energy produced by oscillation of an electric charge.
- **Message signal** - any signal that contains information; it is also called the intelligence signal.
- **Audio Frequency (AF)** - frequencies that a person can hear. AF signals range from about 20 Hz to 20 kHz.
- **Radio Frequency (RF)** - the transmission frequency of electromagnetic (radio) signals. RF frequencies are from about 300 kHz to the 1,000,000 kHz range.
- **Carrier signal** - a single, high-frequency signal that can be modulated by a message signal and transmitted.

- **Modulation** - the process of combining the message signal with the carrier signal that causes the message signal to vary a characteristic of the carrier signal.
- **Demodulation** - the process of recovering or detecting the message signal from the modulated carrier frequency.
- **Amplitude Modulation (AM)** - the process of combining the message signal with the carrier signal and the two sidebands: the lower sideband and the upper sideband.
- **Frequency Modulation (FM)** - the process of combining the message signal with the carrier signal that causes the message signal to vary the frequency of the carrier signal.
- **Phase Modulation (PM)** - the process of combining the message signal with the carrier signal that causes the message signal to vary the phase of the carrier signal.
- **Angle modulation** - the process of combining the message signal with the carrier signal that causes the message signal to vary the frequency and/or phase of the carrier signal.
- **Balanced modulator** - an amplitude modulator that can be adjusted to control the amount of modulation.
- **Double-Sideband (DSB)** - an amplitude modulated signal in which the carrier is suppressed, leaving only the two sidebands: the lower sideband and the upper sideband.
- **Mixer**- an electronic circuit that combines two frequencies.
- **Phase detector** - an electronic circuit whose output varies with the phase differential of the two input signals.
- **Envelopes**- the waveform of the amplitude variations of an amplitude modulated signal.
- **Sidebands** - the frequency bands on each side of the carrier frequency that are formed during modulation; the sideband frequencies contain the intelligence of the message signal.
- **AM** - an amplitude modulated signal that contains the carrier signal and the two sidebands: the lower sideband and the upper sideband.
- **Bandwidth** - the frequency range, in hertz (Hz), between the upper and lower frequency limits.
- **Harmonics** - signals with frequencies that are an integral multiple of the fundamental frequency.

Chapter 2

Tuned Amplifier using IFT

Aim

To design and implement a tuned frequency amplifier using BJT and IFT.

Theory

Intermediate frequency amplifiers are tuned voltage amplifiers used to amplify a particular frequency. Its primary function is to amplify only the tuned frequency with maximum gain and reject all other frequencies above and below this frequency. This type of amplifiers are widely used in intermediate frequency amplifiers in AM super heterodyne receivers, where intermediate frequency is usually 455 kHz.

In common emitter voltage amplifier circuit (emitter bypassed), the voltage gain is $A_V = \frac{R_C||R_L}{r_e}$, where R_C is the collector resistance in the circuit, R_L is the load resistance and r_e is the internal emitter resistance. In tuned voltage amplifier the collector resistance is replace by a tuned load upon which the gain is dependant. For a parallel resonating circuit cosisting of a capacitor, C and an inductor,L the impedance Z_o is maximum at resonant frequency, $f_o = \frac{1}{2\pi\sqrt{LC}}$. So an amplifier with tuned load will have maximum gain at resonant frequency. In practical tuned amplifier circuits, an intermediate frequency transformer(IFT) is used as tuned load. IFT is tuned to standard 455 kHz audio frequency, (See A.1).

The quality factor of the circuit is given by $Q = \frac{f_o}{Bandwidth}$.

Design

Inorder to design a common emitter amplifier operating at high frequency, one can use a high frequency transistor like BF194, BF195, BF494, BF495 or 2N2222.

Choose transistor BF 194/195. For its datasheet See A.2,

Let V_{CC} be 10% more than the required output amplitude, ie. 10V.

$$\therefore V_{CC} = 12\ V \tag{2.1}$$

$$I_c < 10\%\ of\ I_{Cmax} = \ 10\%\ of\ 30\ mA = \ 3mA \tag{2.2}$$

Let $I_c = \ 1mA$. Let the stability factor of the circuit be,

$$S = 10 \tag{2.3}$$

Under dc conditions, the primary dc resistance of the IFT is very small($< 5\Omega$). So dc voltage drop across collector circuit is very low, approximately zero. For class A mode of operation set,

$$V_{CE} = \frac{V_{CC}}{2} = 6V \tag{2.4}$$

Design of Emitter resistance
The voltage across emitter resistance is,

$$V_{RE} = V_{CC} - V_{CE} = \ 12V - \ 6V = \ 6V \tag{2.5}$$

$$I_E \approx I_C \tag{2.6}$$

Hence

$$I_E = 1mA \tag{2.7}$$

Thus

$$R_E = \ \frac{V_{RE}}{I_E} = \ \frac{6V}{1mA} = \ 6k\Omega \tag{2.8}$$

Choose standard value of $R_E = \ 5.6\ k\Omega$.

Design of Potential divider biasing

The Stability factor S=10. Assuming R_B is the effective resistance at the base,

$$S = \ 10 = \ 1 + \frac{R_B}{R_E} \tag{2.9}$$

$$R_B = \ 9R_E = \ 50.4k\Omega \tag{2.10}$$

$$R_B = \ R_1||R_2 = \ \frac{R_1 R_2}{R_1 + R_2} = \ 50.4k\Omega \tag{2.11}$$

The voltage at the base of the transistor is

$$V_B = \ V_E + \ V_{BE} = \ V_{RE} + \ V_{BE} = \ 6V + \ 0.6V = \ 6.6V \tag{2.12}$$

This is the voltage across R_1.

$$V_{R1} = V_{CC}\frac{R_2}{R_1 + R_2} = \ 6.6V \tag{2.13}$$

$$\frac{R_2}{R_1 + R_2} = \frac{6.6V}{12V} = 0.55 \tag{2.14}$$

From equations 2.11 and 2.14,

$$R_1 = 91.4\ k\Omega \approx 82\ k\Omega\ and\ R_2 = 100\ k\Omega \tag{2.15}$$

Choose load resistor as

$$R_L = 100k\Omega \tag{2.16}$$

Design of capacitors

The capacitors C_1, C_2 and C_E can be designed based on lower cut-off frequency at -3 dB point. Since this frequency is much lower than 300 kHz, Choose low values of capacitance like

$$C_1 = C_2 = C_E = 1\ \mu F \tag{2.17}$$

Circuit Diagram

See Figure 2.1 for circuit diagram.

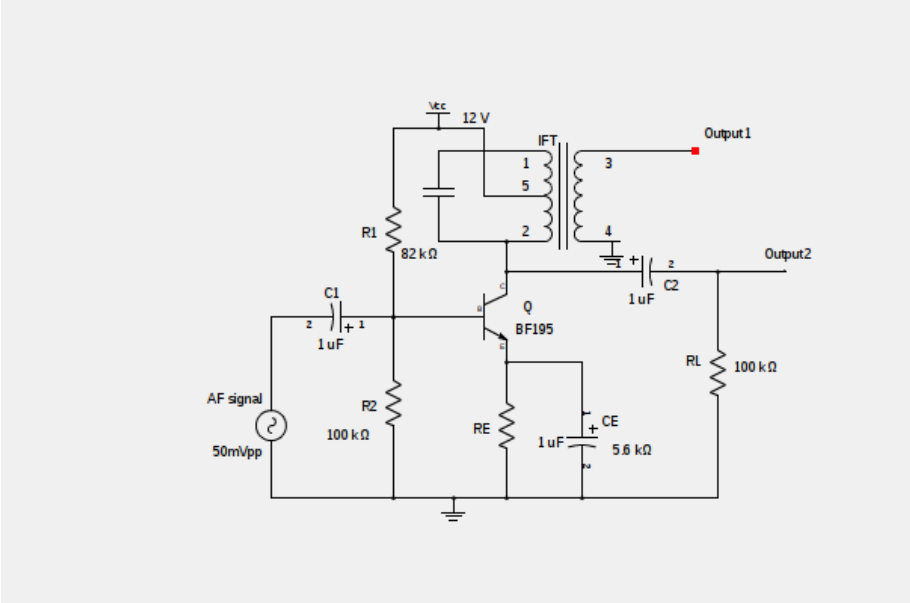

Figure 2.1: Circuit Diagram for IF Tuned Amplifier

Procedure

- Assemble the circuit as shown in the circuit diagram.
- Obtain output from output-1 or output-2 terminal as in the circuit diagram.
- Give input signal, which is a sinewave of frequency variable from 300 kHz to 600 kHz and amplitude 50 mV_{pp}.
- Observe the output waveform on a CRO.
- Enter the details of input and output waveforms on the tabular column shown.
- Calculate gain A_V by varying f_{in}.($A_V = \frac{V_{outpp}}{V_{inpp}}$)
- Plot frequency response characteristics with $f_{in}(kHz)$ along x-axis and $Gain_{dB} = 20\ log\ A_v$ along y-axis.
- Find the resonant frequency, 3-dB bandwidth and hence the Q-factor.

Observation

$f_{in}(kHz)$	$log_{10}\ f_{in}$	$V_{outpp}(V)$	$A_v = \frac{V_{outpp}}{V_{inpp}}$	$Gain_{dB} = 20\ log\ A_v$

Result

A tuned amplifier was implemented using IFT.
Its maximum gain=
Resonant frequency, f_0=
Band-width, BW =
Q-factor=$\frac{f_0}{BW}$

Chapter 3

AM generation using IFT

Aim

To design and set-up an AM generator using BJT and IFT and measure the modulation index from the observed output waveform.

Theory

Any amplifier can be converted into a sinusoidal oscillator if Barkhausen conditions are satisfied. So tuned amplifier in chapter 2 can be converted ito a high frequency oscillator for generating carrier wave by providing a positive feedback after removing the input and the load resistor R_L.

Inorder to obtain the feedback signal to the base, the terminal-1 of the IFT primary coil is used. It is 180° out of phase with the signal at collector, ie. terminal-2 of IFT primary winding. The collector signal is already 180° out of phase with the input signal at base of BJT. Thus the feed back signal from terminal-1 of the IFT to the base of BJT is in phase with the signal at the base. The feedback capacitor is chosen to be low to avoid additional phase shift.

The circuit now works as an oscillator generating a signal of frequency of around 455 kHz. Its amplitude, E_c can be adjusted by varying the potentiometer connected in series with the emitter resistance and frequency, f_c by tuning the IFT.

$$e_c \;=\; E_c \; sin(2\pi f_c t) \tag{3.1}$$

The carrier thus generated can be modulated using an audio frequency message signal by connecting it at the emitter of the transistor. It can be of frequency varying from 1kHz to 5 kHz. The amplitude can be varied in the rage of 1 V to 10 V which changes the modulation index. The modulation index can also be varied by adjusting the carrier amplitude with the potentiometer connected at the emitter.

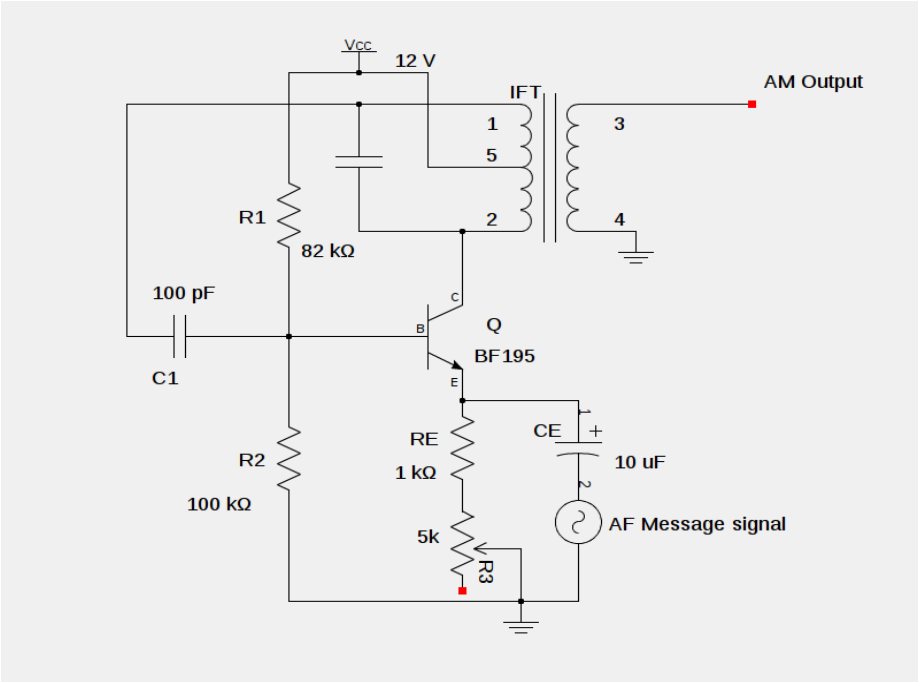

Figure 3.1: Circuit Diagram for AM generation using IFT

The ratio of the maximum amplitude of the modulating signal voltage to that of the carrier voltage is termed as modulation index. This is represented as $m = \frac{E_m}{E_c}$. For both carrier and message being sinusoidal, the modulation index will be $m = \frac{E_{max} - E_{min}}{E_{max} + E_{min}}$ where E_{max} and E_{min} are respectively the maximum and minimum height of the positive side of modulated signal.

Design

The basic biasing of the transistor is as discussed in the chapter 2.
To make the circuit an oscillator, remove input signal and the load.
Positive feed back signal to base is taken from terminal-1 of IFT and given to base through a small capacitance of $C_1 = 100pF$.
The emitter resistance can be raplaced with a fixed resistance of $R_E = 1k\Omega$ in series with a potentiometer of $R_3 = 5k\Omega$.
The modulating signal is connected through a capacitor of $C_E = 10\mu F$.

Circuit Diagram

The circuit diagram is shown in Fig. 3.1

Procedure

1. Set up the circuit after verifying the condition of components.
2. Feed AF modulating signal (say, $f_m = 1kHz$ and $E_m = 5mV$) using a function generator.
3. Adjust amplitude and frequencies of the AF and carrier signals and observe amplitude modulated waveform on the CRO.
4. Fix f_m and f_c. Note down E_{max} and E_{min} of the AM signal and calculate modulation index according to the formula ,

$$m = \frac{E_{max} - E_{min}}{E_{max} + E_{min}}. \tag{3.2}$$

   Here E_{max} is the maximum of the positive envelope of the carrier and E_{min} is the minimum of the positive envelope of the carrier.
5. Repeat for different values of E_m and E_c. Observe the AM waveforms for different values of m.
6. Plot the waveforms on a graph sheet.
7. Fill in the observation column

Observation

Figure. 3.2 shows the effect of modulation index on the resultant AM wave[1]

E_{min}	E_{max}	$m = \frac{E_{max}-E_{min}}{E_{max}+E_{min}}$

Result

Implemented the AM modulation circuit using BJT and IFT. Tabulated the modulation index by varying the amlitudes of message and the carrier.

[1] Image source: https://commons.wikimedia.org:/wiki/File:Amplitude_Modulated_Wave-hm-64.svg

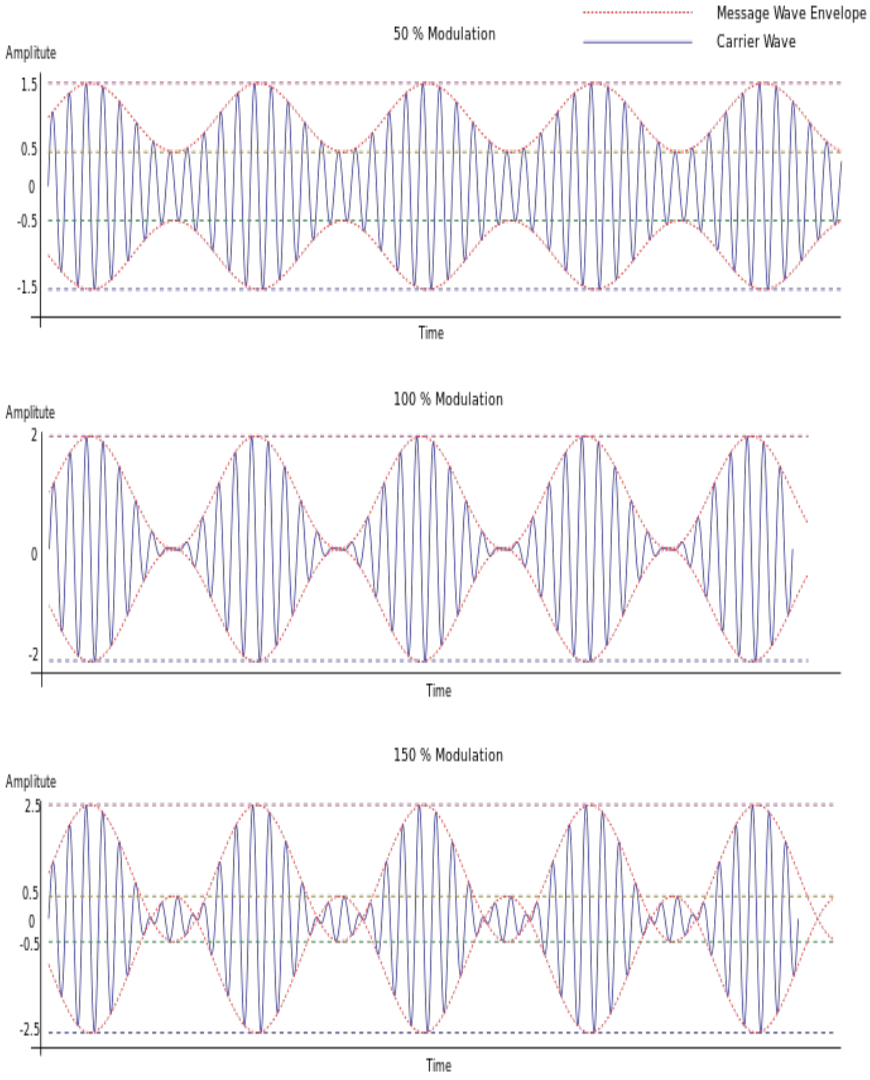

Figure 3.2: Effect of modulation index on AM

Chapter 4

AM Detection with Automatic Gain Control

Aim

To demodulate the message content from AM signal. Also detect the automatic gain control signal from the received AM signal.

Theory

A simple AM demodulator is a diode envelope detector. It can be implemented by a simple diode envelope detector to eliminate the negative half of the carrier envelope followed by a simple RC filter to remove the high frequency carrier. The result will be the low frequency envelope which is the demodulated message.

A point contact diode with low junction capacitance is used in the circuit as it is has to rectify high frequency carrier. It offers low impedence at high frequency. The RC elements connected after the diode acts as a filter. It acts as a lowpass filter which eliminates high frequency carrier at the same time it retains the low frequency message signal.

Thus the output of the filter contains the low fequency modulating signal with a dc offset. The dc offset voltage is proportional to the strength of the modulated signal received by the receiver in a transmission reception system, which inturn is proportional to the strength(amplitude) of the carrier. This dc value may be used for automatic gain control(AGC) of intermediate frequency(IF) amplifier stages. The Automatic gain control compensates for minor variations in the received RF signal level. The AGC circuit automatically increases the receiver gain for weak RF input levels and automatically decreases the receiver gain when strong RF signal is received[1].

[1] For detailed explanation, refer to Chapter 5 of [3]

Simple AGC: It is implemented in the form of a circuit which extracts the dc offset voltage which is present along with the demodulated message. This volatge is fed as degenerative or negtive feedback to the control the gain of superheterodyne receivers.

Delayed AGC: In simple AGC circuits even if the signal level received is low, the AGC circuit operates and the overall gain of the receiver gets reduced. To avoid this situation, a delayed AGC circuit is used. In this case AGC bias voltage is not applied to amplifiers, until signal strength has reached a predetermined level after which AGC bias is applied like simple AGC.

Design

After the positive envelope detector, a properly designed low pass filter is added to filter out the high frequency carrier and to retain the low frequency modulating signal. This signal contains a dc level also which can be used for automatic Gain Control (AGC) for the IF amplifier stages of a superhetrodyne receiver.

Let the carrier frequency be $f_c = 455\ kHz$ and maximum modulating signal frequency be $f_m = 10\ kHz$
Inorder to design a lowpass filter with upper cutoff frequency 10 kHz,

$$f_H = \frac{1}{2\pi R_d C_d} \tag{4.1}$$

$$10\ kHz = \frac{1}{2\pi R_d C_d} \tag{4.2}$$

Select $C_d = 0.001\mu F$. Then $R_d = 16.1k\Omega$. Choose $R_d = 15k\Omega$ *or* $22k\Omega$ standard resistor values.

Make a π filter (for better performance) using these R_d and C_d values. This completes the envelope detector part.

AGC Circuit: The AGC lowpass filter R_a and C_a is seected in such a way as to eliminate full ac from the output and get a pure dc AGC voltage. Hence assuming a cutoff frequency of 10 Hz to eliminte the fluctuations,

$$10Hz = \frac{1}{2\pi R_a C_a} \tag{4.3}$$

Assuming $C_a = 1\mu F$, we get $R_a = 22k\Omega$

The actual modulating signal can be obtained by filtering out the dc components using a high value caacitance like $10\mu F$.

Circuit Diagram

The detector circuit with simple AGC is shown in Figure. 4.1.

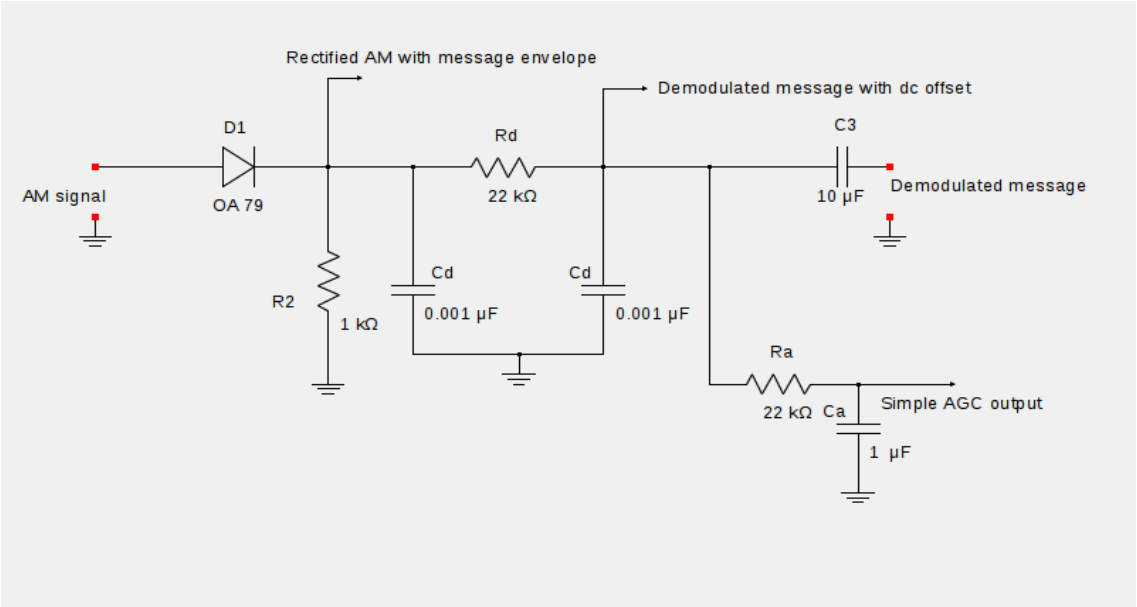

Figure 4.1: Detector circuit with Simple AGC

Procedure

1. Connect the diode to the output of AM signal(See Figure. 4.2) as in the circuit diagram Fig. 4.1.

2. Connect load resistance R_L and observe the outputwaveform on a CRO and plot it.

3. Connect the π filter circuit of R_d and C_d and observe the output waveform on a CRO and plot it.

4. Obtain the demodulated output without dc offset by connecting capacitor C_3. Observe it on a CRO and plot it.

5. Connect the lowpass filter using C_a and R_a for obtaining AGC voltage level. Observe it on a CRO and plot it.

6. Vary the modulation index by changing carrier or modulating signal levels. Plot the simple AGC charateristics with modulation index on x-axis and AGC voltage level on y-axis.

7. Eliminte the dc offset and observe the modulating signal from the $10\mu F$ capacitor as shown in the circuit diagram.

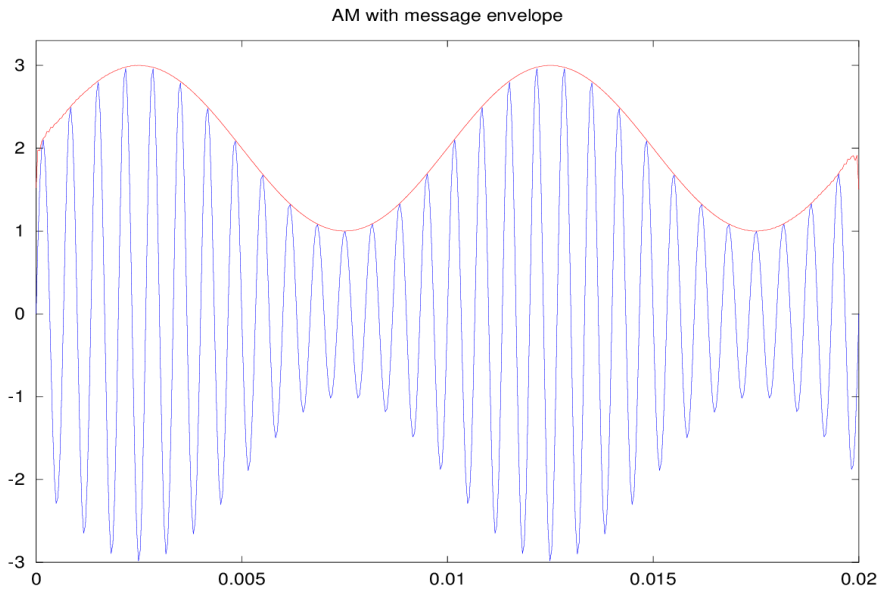

Figure 4.2: AM with message envelope

Observation

The following are the observed results of the experiment. See Figure. 4.3 and Figure. 4.4 for the waveforms of intermediate and final stages.

Result

Demodulation circuit was designed and implemented with simple AGC.

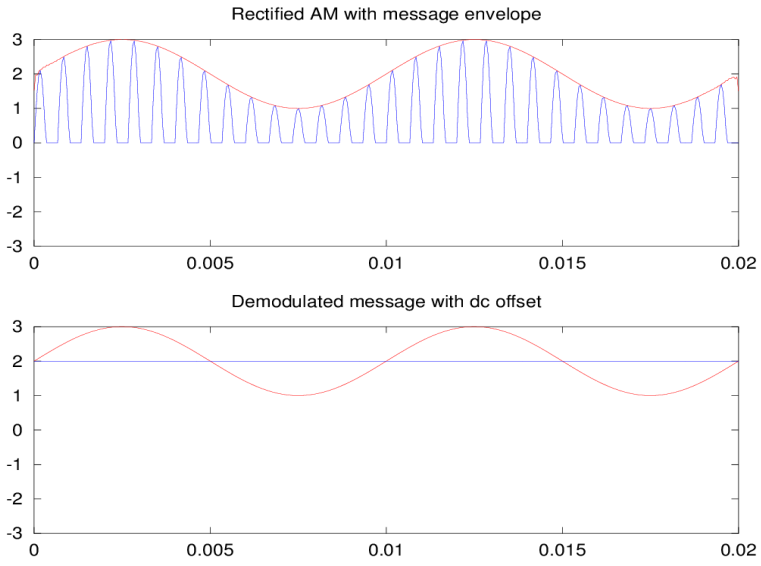

Figure 4.3: Intermediate stage of demodulation

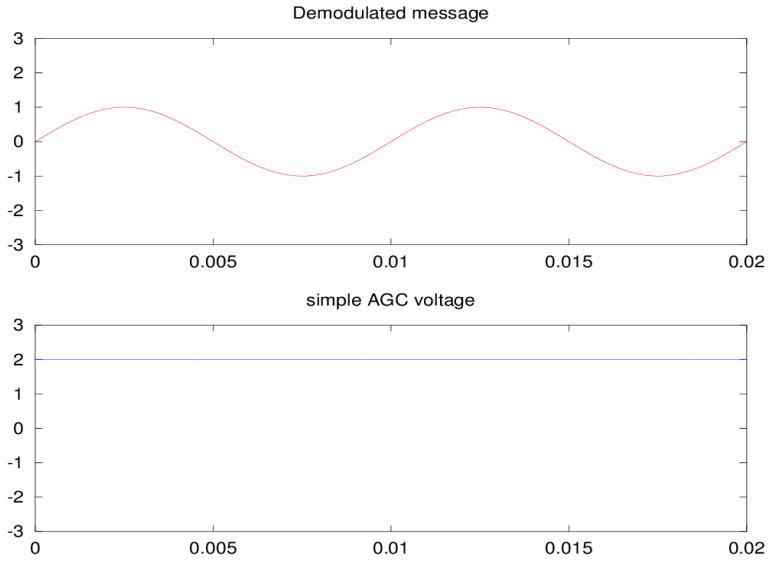

Figure 4.4: Output waveforms from demodulation circuit

Chapter 5

PAM Generation and Demodulation

Aim

To set-up and implement circuits to carry out pulse amplitude modulation. To design demodulationg circuits to detect the message from pulse amplitude modulated wave.

Theory

Pulse amplitude modulation is a kind of digital modulation technique in which analog message signal is sampled at constant frequency - *carrier frequency*. A pulse of specified duration is used to sample the message signal. When the pulse is on, the message is sampled and when it is off no message is sampled. This is a basic step in the digitization of analog message signals. The circuits to be implemented in this experiment does a kind of natural sampling.[1].

Waveforms showing pulse carriers whose amplitude is modulated buy message is shown in Figure 5.1 and **??**. A simple way to implement this is to allow the message to be fed as the input to a switch and the switch ON/OFF time is controlled by the pulses at sampling frequency.

The demodulation of PAM waveform can be implemented by using a lowpass filter which passes message signal frequenies but blocks the carrier signal.

[1] For more on natural sampling, refer Digital Transmission [3]

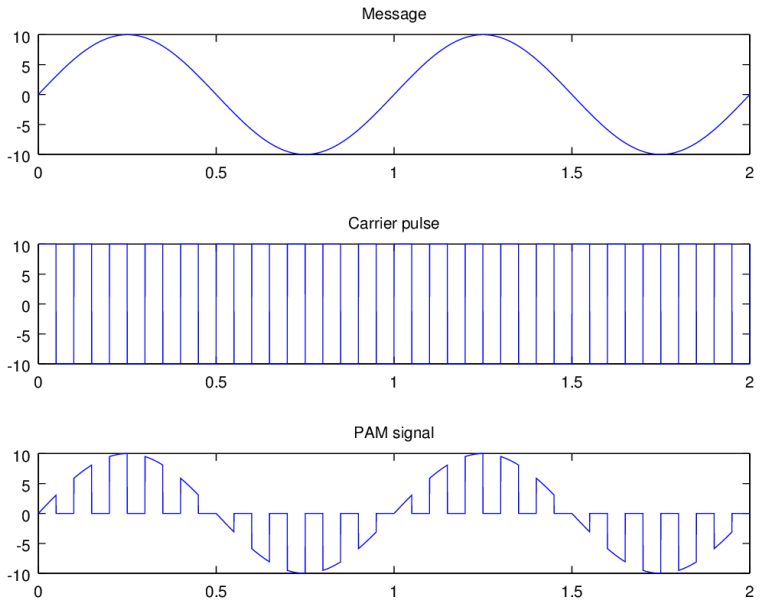

Figure 5.1: PAM modulation using transistor

Design

PAM using transistor as a switch

One technique to implement PAM is to use transistr in switching mode. The flow of current from collector to emitter in a bipolar junction transistor is controlled by the voltage at its base.
Choose the transistor BC107. For more details on BC107 see A.3. Apply the sinusoidal message signal of frequency $f_m < 1\ kHz$ and amplitude $E_m < 10\ V_{pp}$ at the collector. Apply a carrier at the transistor base through a resistor $10k\Omega$. The carrier pulse amplitude is set as $E_c = 10\ V_{pp}$ and frequency $f_c = 10kHz$.

PAM using CMOS switching IC CD4016

CD 4016 is a quad bilateral CMOS switching IC. See A.4 for more deatails. The message signal is fed to any of the input terminals of the switch and the modulating pulse carrier is fed as the control signal for the switch. The PAM output will be available at the output terminal of the switch which is fed to the CRO across a load resistor of 10 $k\Omega$. Keep the message signal frequency to be $f_m = 500\ Hz$ and the switching pulse of 10 kHz which is the carrier is to be fed from the TTL output from a function generator.

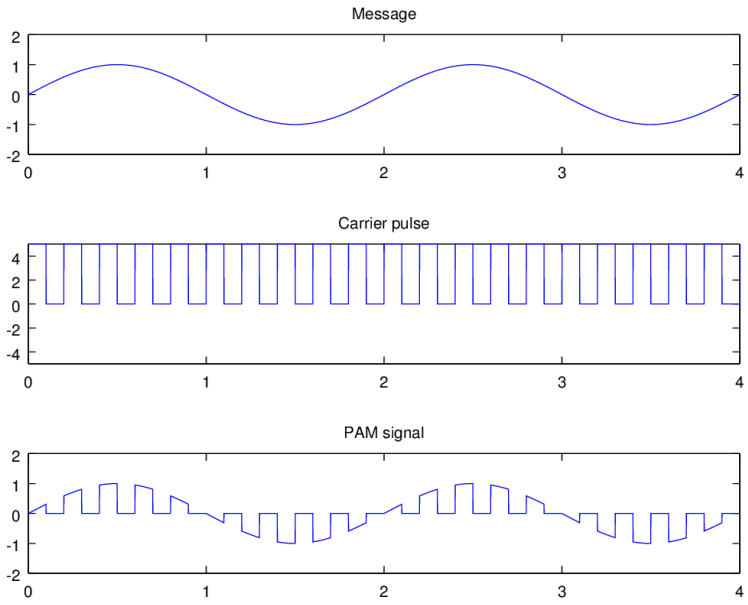

Figure 5.2: PAM modulation using switching IC

Demodulation

Demodulation is done using a π RC filter. Design the filter as per the equation for upper cut-off frequency of a low pass filter,

$$f_H = \frac{1}{2\pi R_d C_d} \tag{5.1}$$

$$1.5\ kHz = \frac{1}{2\pi R_d C_d} \tag{5.2}$$

Select $C_d = 0.01\mu F$. Then $R_d = 10k\Omega$. Choose $R_d = 10k\Omega$ standard resistor value.

Circuit Diagram

Using transistor as a switch

The PAM generation using transistor as a switch and demodulation circuit is shown in Figure. 5.3.

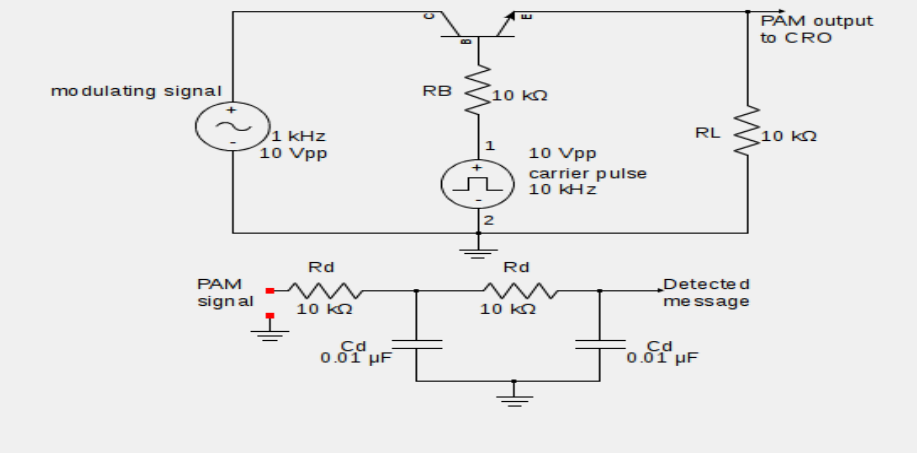

Figure 5.3: PAM generation and demodulation circuuit

Using CMOS switching IC CD4016

The PAM generation using CD4016 is shown in Figure. 5.4. Demodulation can be done in the same way as shown in 5.3.

Procedure

- Connect the PAM generating circuit as shown in the circuit diagram, Figure 5.3.
- Feed the modulating message signal and the carrier pulses from the function generator.
- Observe the output on a CRO and plot the graphs of the input and output waveforms.
- Make the demodulating circuit as shown in the circuit diagram, Figure 5.3.
- Repeat the PAM experiment using CD4016 IC.
- Make connections as shown in the circuit diagram Figure. 5.4. If IC is used for modulation make sure it is biased with $V_{DD} = 5V$ and is properly grounded.
- Observe the input and output waveforms from PAM generaton and demodulation circuits using CD4016 IC.

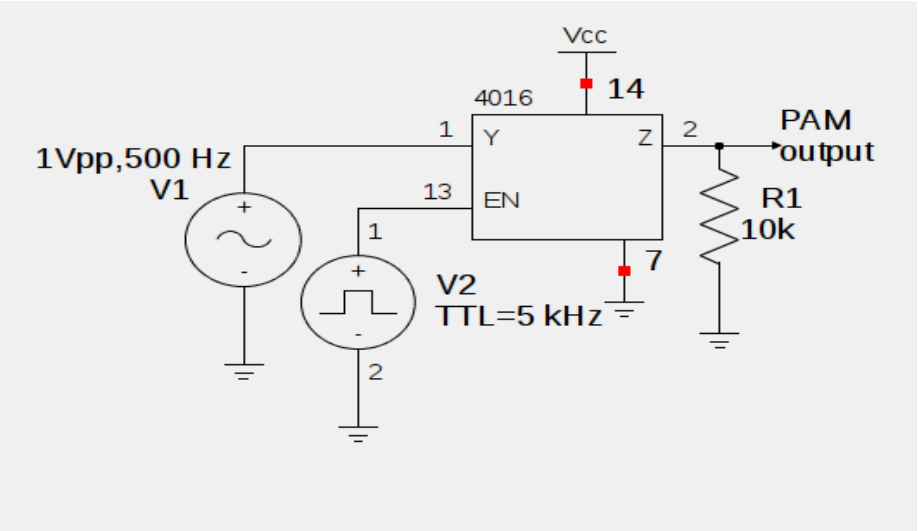

Figure 5.4: PAM generation using CD4016

Observation

Plot the graphs of input and ou tput waveforms as observed on a CRO.

Result

Implemented the PAM generation and demodulation circuits using BJT as well as switching IC.

Chapter 6

DSB-SC using multiplier IC AD633

Aim

To set up a balanced modulator circuit for double side band suppressed carrier amplitude modulator.To implement a demodulator to obtain the message signal.

Theory

DSB-SC is a kind of amplitude modulation in which the carrier frequency component is absent. It is generated by multiplying the carrier and modulating signals. If e_c is the carrier and $e_m$is the message signal, where

$$e_c = E_c \ sin \ 2\pi f_c t \tag{6.1}$$

$$e_m = E_m \ sin \ 2\pi f_m t \tag{6.2}$$

Multiplication is done using AD633 (See A.5) multiplier IC. Applying e_m to **X** and e_c to **Y** with **Z** grounded,

$$W = \frac{e_m e_c}{10} = \frac{Emsin(2\pi f_m t).Ecsin(2\pi f_c t)}{10} \tag{6.3}$$

$$W = \frac{E_m E_c}{10} \frac{[cos2\pi(f_c \ - \ f_m)t - cos2\pi(f_c \ + \ f_m)t]}{2} \tag{6.4}$$

$$W = \frac{E_m E_c[cos2\pi(f_c \ - \ f_m)t]}{20} - \frac{E_m E_c[cos2\pi(f_c \ + \ f_m)t]}{20} \tag{6.5}$$

This wave contains both the sidebands at $f_c - f_m$ and $f_c + f_m$, but not the wave at carrier frequency[1]. Hence the name double sideband suppressed carrier modulation(DSB-SC).

[1] $sin \ A. \ sin \ B = \frac{cos \ (A-B) - cos \ (A+B)}{2}$

The following figure 6.1 shows[2] the DSB-SC signal in blue and the original message is shown in red. (*It is an indicative graph, not to scale as per the experimental set-up.*)

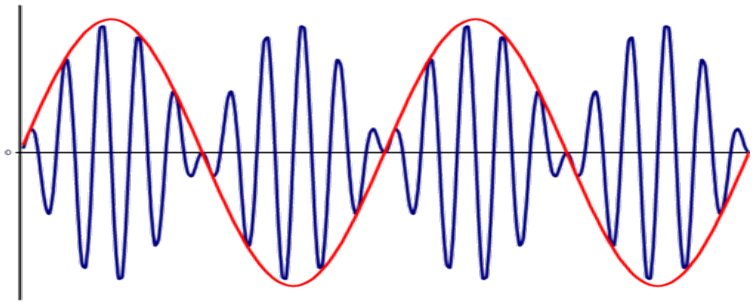

Figure 6.1: DSB-SC signal in blue, original message shown in red.

Multiplying the DSB-SC with the carrier once again will result in the following output.

$$W = \frac{1}{10}[\frac{E_m E_c[cos(2\pi(f_c - f_m)t)]}{20} - \frac{E_m E_c[cos(2\pi(f_c + f_m)t)]}{20}].E_c sin(2\pi f_c t) \tag{6.6}$$

$$W = \frac{E_m.{E_c}^2}{400} sin(2\pi(2f_c - f_m)t) - \frac{E_m.{E_c}^2}{400} sin(2\pi(2f_c + f_m)t) + \frac{E_m.{E_c}^2}{200} sin(2\pi f_m t) \tag{6.7}$$

Thus the signal consists of various frequencies of which, the smallest is the message frequency. It can be extracted by filtering using a low pass filter. Since the amplitude of the message frequency is very small, It may be amplified using a simple non-inverting amplifier using an opamp.

Design

To the **X** input of the IC, feed the message sinusoid of amplitude $E_m = 2.5\ V$ (ie., peak to peak amplitude of 5 V) and frequency $f_m = 1\ kHz$.

To the **Y** input of the IC, feed the carrier sinusoid of amplitude $E_c = 2.5\ V$ and frequency $f_c = 100\ kHz$.
Ground the **Z** input of the IC.

[2]Image Courtesy: Serych at cs.wikipedia [Public domain], from Wikimedia Commons

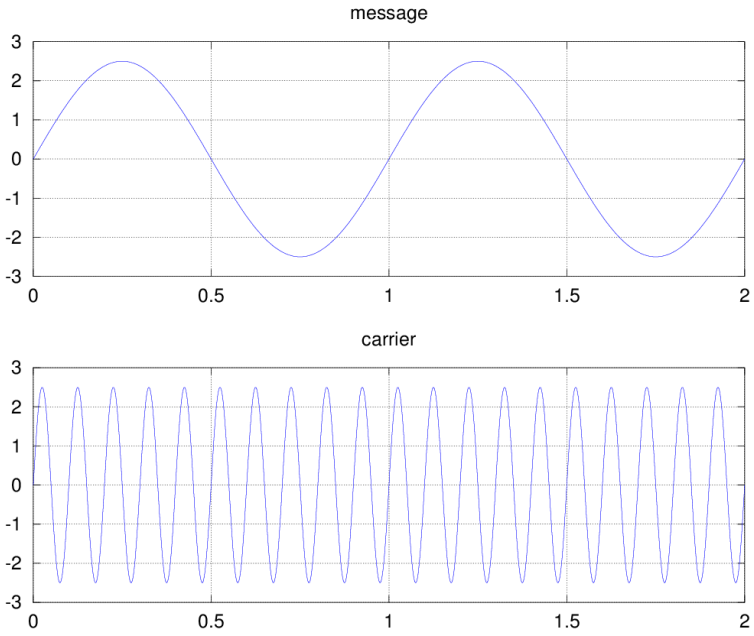

Figure 6.2: Message and carrier signals

Provide the supply voltage of **+15 V to pin 8** of the IC and **-15 V to pin 5** of the IC.

The output signal will have a waveform as given by,

$$W = \frac{X.Y}{10} + Z \tag{6.8}$$

$$W = \frac{e_m.e_c}{10} = \frac{(2.5)\ .(2.5)}{10}\frac{[cos2\pi 99kt - cos2\pi 101kt]}{2} \tag{6.9}$$

$$W = \frac{6.25}{20}[cos2\pi 99kt - cos2\pi 101kt] \tag{6.10}$$

This is the DSB-SC waveform.

Demodulation is by multiplying the DSB-SC signal once again with the carrier. This can be implemented by connecting another AD633 IC in cascade with the first one.
The multiplication will result in the following output, as per the theory already explained.

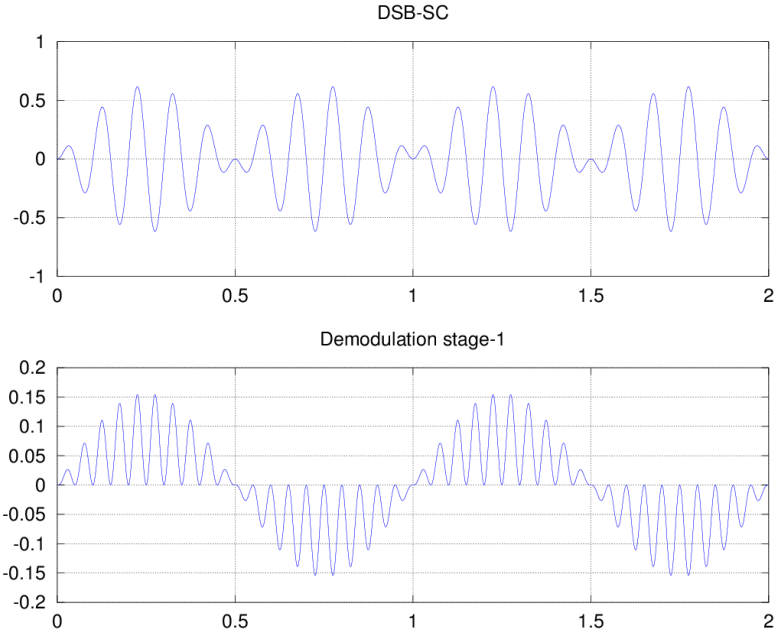

Figure 6.3: AM(DSB-FC) and Demodulation stage-1 signals

$$W = \frac{15.625}{200} sin(2\pi 1kt) + \frac{15.625}{400} sin(2\pi 199kt) - \frac{15.625}{400} sin(2\pi 201kt) \tag{6.11}$$

This waveform is shown in Figure 6.3, which is the stage -1 in demodulation. The next step is to obtain the message signal. This is done by lowpass filtering the above signal at a cut-off frequency of 1.5 kHz.

To design an RC lowpass filter of cut-off frequency 1.5 kHz,

$$f_c = \frac{1}{2\pi R_1 C_1} = 1.5kHz \tag{6.12}$$

Choose $C_1 = 0.01\ \mu F \therefore R_1 = 10\ k\Omega$

A non-inverting amplifier may be used to amplify this signal. Using a feedback resistor of $R_f = 100\ \Omega$ and an input resistance of $R_i = 10\ k\Omega$ will result in a gain of $A_v = 1 + \frac{R_f}{R_i} = 11$.

Circuit Diagram

The circuit diagram for implementing DSBSC using multiplier IC is shown in figure 6.4.

Procedure

- Make connections as shown in the circuit diagram, figure 6.4.
- Feed the message and carrier signals.
- Connect the pin number 7 of the IC to a CRO and observe the resultant waveform which is DSB-SC.
- Connect the pin number 7 of the second IC to a CRO and observe the resultant waveform which is the product of DSB-SC and the carrier.(Named demodulation stage-1 signal)
- Observe the output from the filter, amplified by the opamp amplifier, which extracts the envelope -*The 1kHz message signal*- of the previous signal.
- Plot the signals observed on a graph sheet.

Observation

The input and output signals as observed on a CRO are shown in Figure 6.2 and 6.3.

Result

Implemented DSB-SC using multiplier IC AD 633 and observed the signal waveforms.

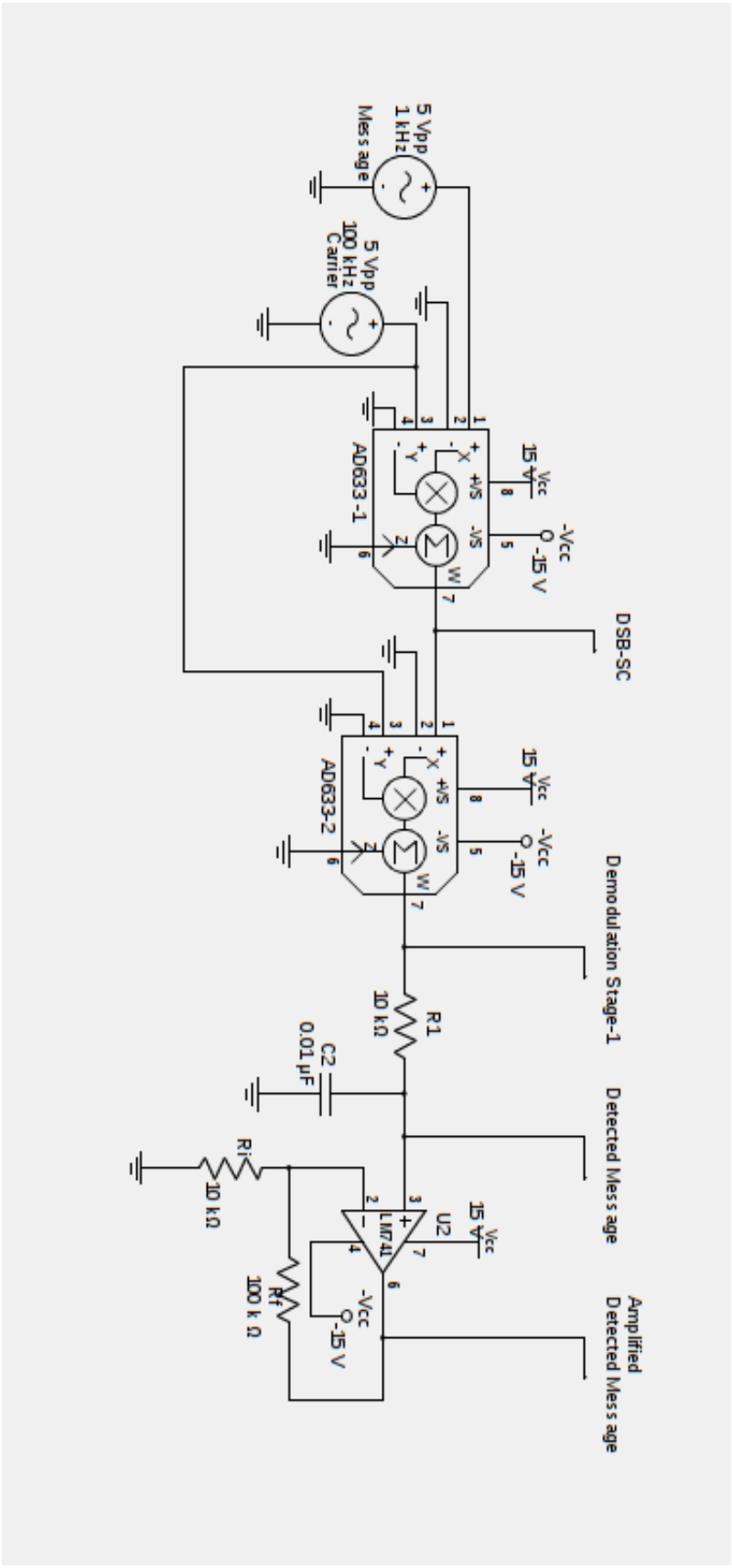

Figure 6.4: Circuit for DSB-SC generation and detection using AD633 multiplier IC

Chapter 7

AM generation and Demodulation using AD 633

Aim

To design and implement AM generation and demodulation using multiplier IC AD633.

Theory

DSB-SC using AD633 has already been discussed in chapter 6. DSB-SC is same as AM devoid of the carrier. Inorder to obtain the complete AM waveform which is *double side band with carrier*, add the carrier signal to the DSB-SC signal. This can be done using the 633 multiplier IC. For more details on IC, refer A.5.

$$W = \frac{X.Y}{10} + Z \tag{7.1}$$

$$W = \frac{Emsin(2\pi f_m t).Ecsin(2\pi f_c t)}{10} + E_c sin(2\pi f_c t) \tag{7.2}$$

$$W = \frac{E_m E_c[cos(2\pi(f_c - f_m)t)]}{20} - \frac{E_m E_c[cos(2\pi(f_c + f_m)t)]}{20} + E_c sin(2\pi f_c t) \tag{7.3}$$

The resultant AM can be demodulated in two ways,

1. Using Diode envelope detector.
2. Using another AD633 in cascade with AM generating circuit for multiplying the AM with the carrier.

Multiplying the AM with the carrier once again will result in the following output.

$$W = \frac{1}{10}[\frac{E_m E_c[cos(2\pi(f_c - f_m)t)]}{20} - \frac{E_m E_c[cos(2\pi(f_c + f_m)t)]}{20} + E_c sin(2\pi f_c t)].E_c sin(2\pi f_c t) \tag{7.4}$$

$$\begin{aligned} W =& \frac{{E_c}^2}{20} + \frac{E_m.{E_c}^2}{200} sin(2\pi f_m t) \\ & - \frac{{E_c}^2}{20} cos(2\pi(2f_m)t) \\ & + \frac{E_m.{E_c}^2}{400} sin(2\pi(2f_c - f_m)t) - \frac{E_m.{E_c}^2}{400} sin(2\pi(2f_c + f_m)t) \end{aligned} \tag{7.5}$$

Thus the signal consists of various frequencies of which, the smallest is the message frequency. It can be extracted by filtering using a low pass filter. Since the amplitude of the message frequency is very small, It may be amplified using a simple non-inverting amplifier using an opamp.

Design

Provide the supply voltage of +15 V to pin 8 of the IC and -15 V to pin 5 of the IC.

To the **Y** and **Z** inputs of the IC, feed the carrier sinusoid of amplitude $E_c = 2.5\ V$ and frequency $f_c = 100\ kHz$.
To the **X** input of the IC, feed the message sinusoid of amplitude $E_m = 2.5\ V$ and frequency $f_m = 1\ kHz$.

The output AM signal will have a waveform as given by,

$$W = \frac{X.Y}{10} + Z \tag{7.6}$$

$$W = \frac{e_m.e_c}{10} + e_c \tag{7.7}$$

$$W = \frac{6.25}{20}[cos2\pi 99kt - cos2\pi 101kt] + 2.5sin(2\pi 100kt) \tag{7.8}$$

Thus it contains two sidebands and the carrier, ie *Double sideband - Full Carrier AM.*

Demodulation: Detection may be done using a diode envelope detector as already discussed in chapter 4.

An alternate method of demodulation is by multiplying the AM signal once again with the carrier. This can be implemented by connecting another AD633 IC in cascade with the first one.

The multiplication will result in the following output, as per the theory already explained.

$$\begin{aligned} W =& \frac{6.25}{20} + \frac{15.625}{200} sin(2\pi 1kt) \\ & - \frac{6.25}{20} cos(2\pi 2kt) + \frac{15.625}{400} sin(2\pi 199kt) - \frac{15.625}{400} sin(2\pi 201kt) \end{aligned} \tag{7.9}$$

This waveform is shown in Figure 7.3, which is the stage -1 in demodulation. The next step is to obtain the message signal. This is done by lowpass filtering the above signal at a cut-off frequency of 1.5 kHz.

To design an RC lowpass filter of cut-off frequency 1.5 kHz,

$$f_c = \frac{1}{2\pi R_1 C_1} = 1.5kHz \tag{7.10}$$

Choose $C_1 = 0.01\ \mu F \therefore R_1 = 10\ k\Omega$

A non-inverting amplifier may be used to amplify this signal. Using a feedback resistor of $R_f = 100\ k\Omega$ and an input resistance of $R_i = 10\ k\Omega$ will result in a gain of $A_v = 1 + \frac{R_f}{R_i} = 11$.

Circuit Diagram

The circuit diagram for generating AM(DSB-FC) and demodulating it using AD633 multiplier IC as shown in Figure. 7.1.

Procedure

- Make connections as shown in the circuit diagram, figure 7.1.
- Feed the message and carrier signals.
- Connect the pin number 7 of the first IC to a CRO and observe the resultant waveform which is AM(DSB-FC).
- Connect the pin number 7 of the second IC to a CRO and observe the resultant waveform which is the product of DSB-FC and the carrier.(Named demodulation stage-1 signal)
- Observe the output from the filter, amplified by the opamp amplifier, which extracts the envelope of the signal-*The 1kHz message signal.*
- Plot the signals observed on a graph sheet.

Observation

The input and output signals as observed on a CRO are shown in Figure 7.2and 7.3.

Result

Implented the AM generation and demodulation circuit using multiplier IC and opamps. The resultant waveforms were plotted.

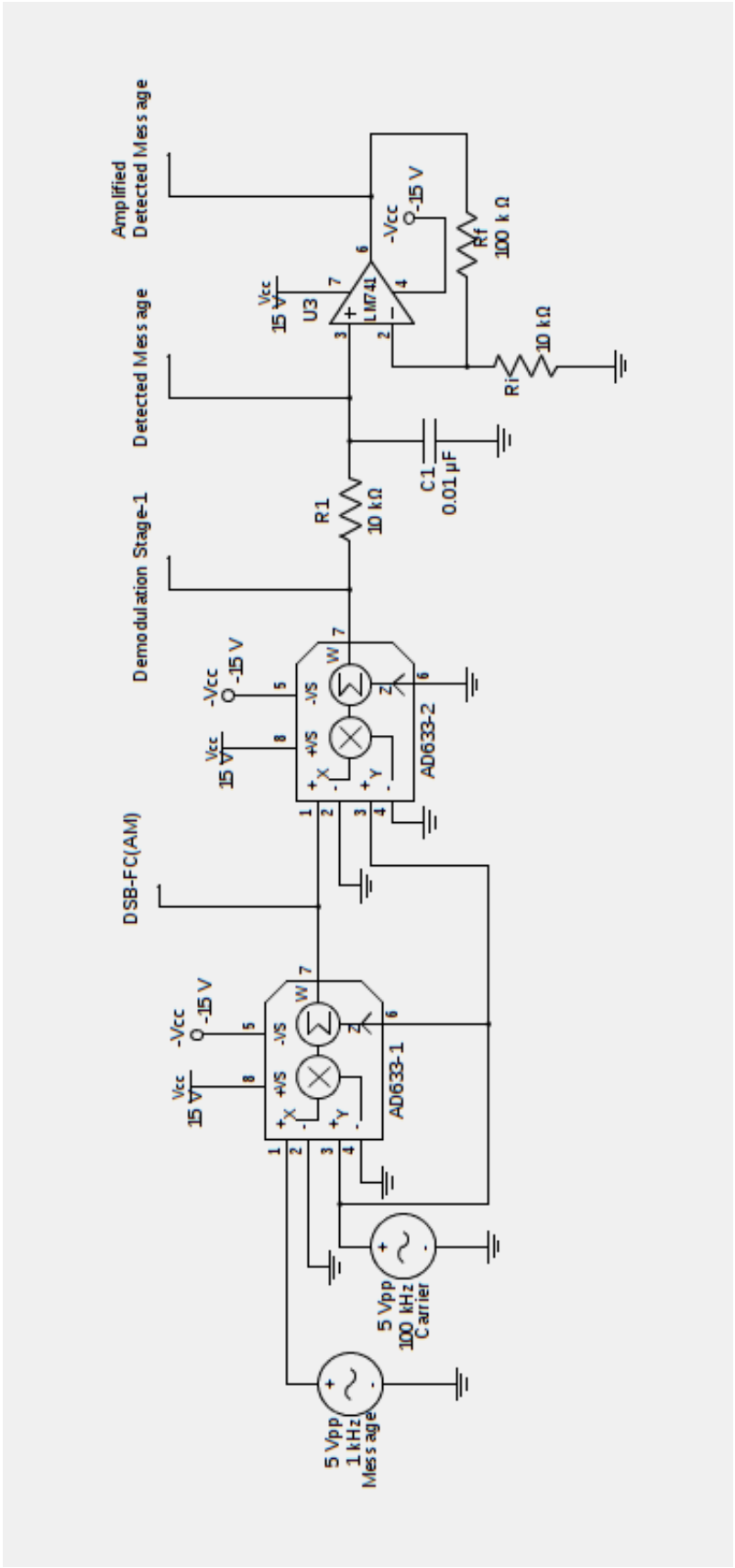

Figure 7.1: Circuit for AM generation and detection using AD633 multiplier IC

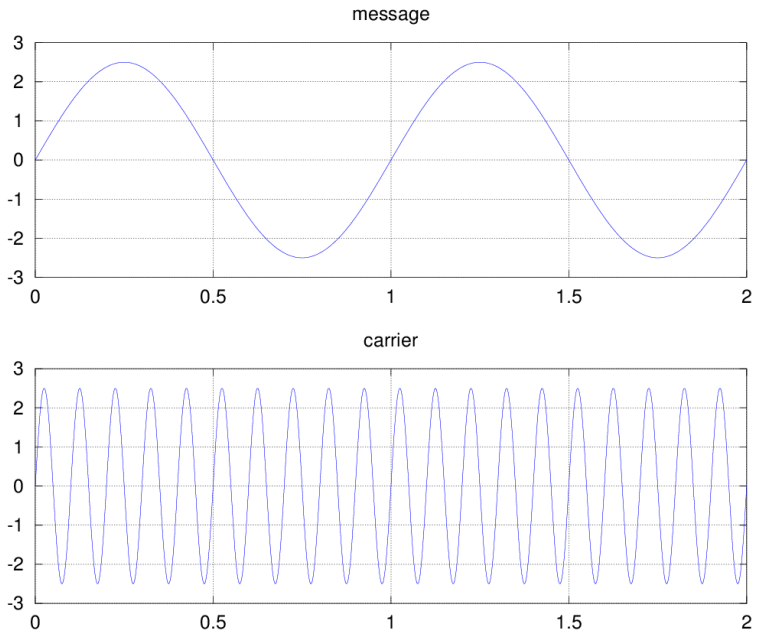

Figure 7.2: Message and carrier signals

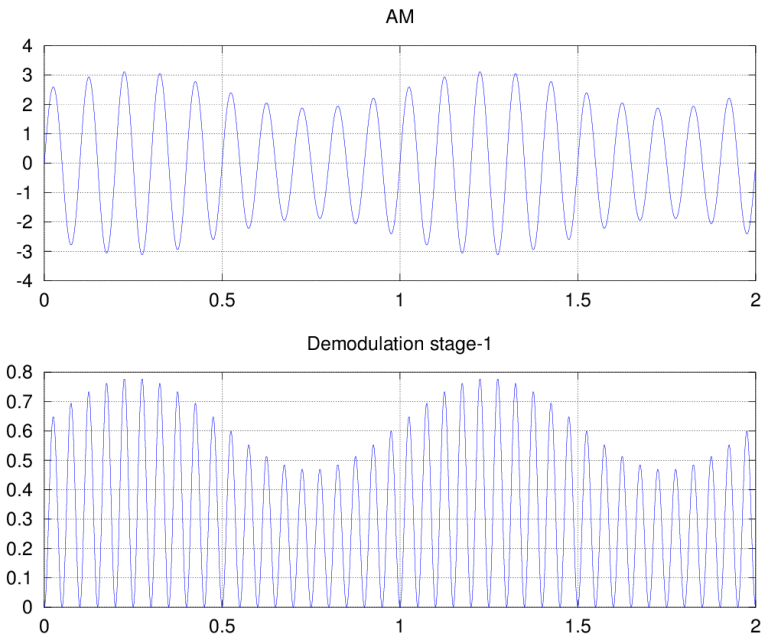

Figure 7.3: AM(DSB-FC) and Demodulation stage-1 signals

Chapter 8

FM using 555

Aim

To design and set up a frequency modulating circuit using 555.

Theory

Frequency modulation is an analog modulation technique in which the frequency of the carrier is varied in accordance with the message signal amplitude. Modulation index for FM is

$$m = \frac{\delta f}{f_m} = \frac{frequency\ deviation}{modulating\ signal\ frequency} \tag{8.1}$$

555 is an IC which can be used to to set up an astable multivibrator of 50% duty cyle whose frequency is determined by externally connected RC load. *(See Appendix A.6)*
The standard design equation for an astable mutivibrator using 555 timer IC is defined by the following equation for its time period.

$$T = 1.38\ RC \tag{8.2}$$

Thus its frequency of oscillation is

$$f_0 = \frac{0.72}{RC} \tag{8.3}$$

This frequency of oscillation remains constant as long as the pin-5 is supplied with a constant voltage. If the voltage at pin-5 is varying the frequency of oscillation of the astable multivibrator also changes along with it.

Thus astable multivibrator using 555 can be used as a carrier pulse generator. The frequency of the carrier can be varied by feeding the pin-5 with message signal.

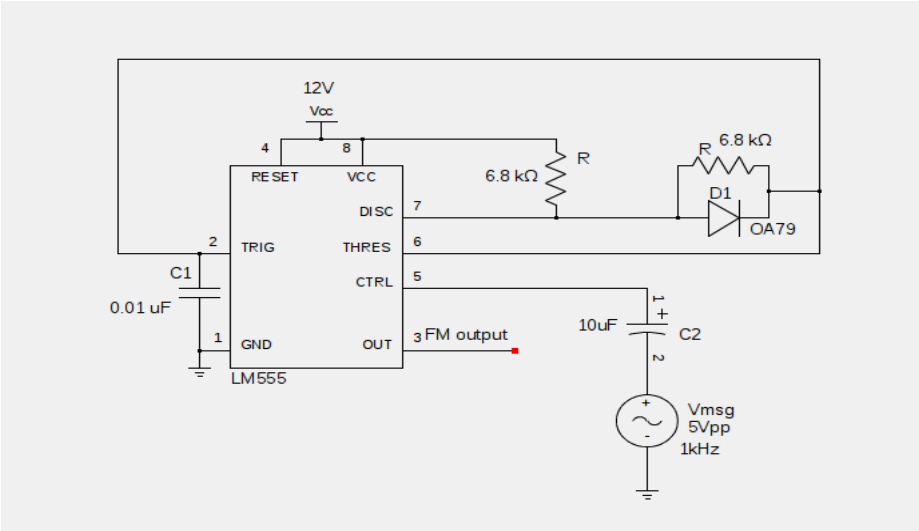

Figure 8.1: Circuit to implement frequency modulation using 555

Design

Let the carrier frequency be given by $f_c = 10kHz$

$$f_c = \frac{0.72}{RC} \tag{8.4}$$

Let $C = 0.01\mu F$

$$\therefore R = \frac{0.72}{(10)(10^3)(0.01X10^{-}6)} = 6.8k\Omega \tag{8.5}$$

The amplitude of the modulationg signal should be limited by $\frac{2}{3}V_{cc}$. This is needed to avoid over modulation. The message signal should have a frequency less than 1 kHz.

The dc supply voltage of the IC,

$$V_{cc} = 12V \tag{8.6}$$

$$\therefore V_{m_{pp}} = \frac{2}{3}X12V = 8V \tag{8.7}$$

Circuit Diagram

The circuit to implement frequency modulation using 555 is shown in Figure 8.1.

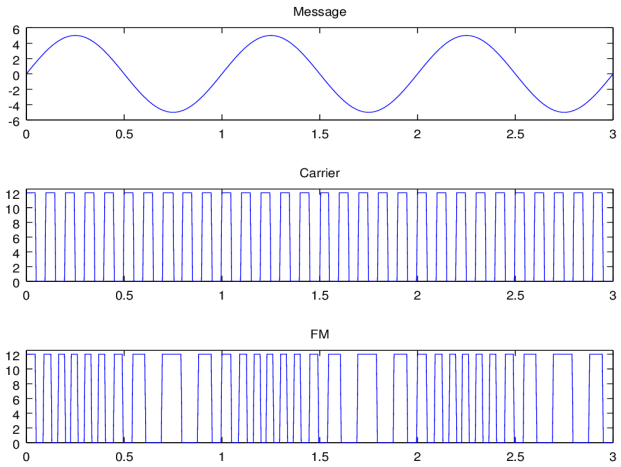

Figure 8.2: Message, Carrier and frequency modulated waveforms

Procedure

- Make connections as per the circuit diagram.
- Feed the message signal of peak-to-peak amplitude of 5V and frequency 1kHz.
- Observe the FM output at pin number-3.
- Plot the observations on a graph sheet.

Observations

Observe the input and output waveforms on a CRO and plot the same on a graph sheet. See Figure 8.2.

Result

Implemented frequency modulation of pulse carrier by sinusoidal messaage using 555 timer IC.

Chapter 9

FM - Modulation and Demodulation using PLL

Aim

To implement FM modulation and demodulation circuits using PLL IC CD4046

Theory

CD 4046 is an analog Phase Locked Loop IC, whose characteristics and features are discussed in Appendix A.7. This IC can be used for FM modulation and demodulation.

FM Modulation

The VCO part of the PLL may be used for the frequency modulation of the carrier. In a VCO, the output frequency is proportional to the control volatge input. In the absance of control voltage, the free running frequency is determined by the supply voltage V_{CC}, the externally connected resistances R_1 and R_2 and the capacitance C. The free running frequency f_0 is given by

$$f_0 = \frac{0.16\ X\ \frac{V_{CC}}{2}}{R_1.C} + \frac{1}{R_2.C} \tag{9.1}$$

The VCO in free running mode is the carrier generator. The carrier frequency is f_0. The control input of the VCO is clamped at a voltage $\frac{V_{cc}}{2}$. The modulating signal voltage which is less than $\frac{V_{cc}}{2}$ is applied at this pin through a capacitor. This results in variation in the frequency of oscillation of the VCO, which is the frequency modulated signal.

FM Demodulation

Another PLL IC has to be used for FM demodulation. The VCO part of this IC is configured for the same free running frequency as that of the modulator IC.

One of the phase detector input is fed with the modulated FM signal and the other input of the phase detector is fed with the VCO output after filtering out high frequency componens. The phase variation between the two will be corresponding to the message which was used for modulation. The PD output is passed through an emitter follower internally to the demodulated output pin. The output from this pin may contain high frequency ripples which may be eliminated by proper filtering to obtain the actual message.

Design

Supply $V_{CC} = 5V$ at pin-16 and ground pin-8 of both PLL ICs.

Modulation Use a voltage divider network of two resistors with $R = 10\ k\Omega$ for clamping the control voltage input (pin-9) at $\frac{V_{cc}}{2} = 2.5V$.
Give a message signal of frequency 1kHz and amplitude 1 V_{pp} at control voltage input (pin-9) throgh a capacitor of $C_1 = 1\mu F$.
Select $R_1 = 10\ k\Omega$ (pin-11), $R_2 = 100\ k\Omega$ (pin-12) and $C = 0.002\mu F$(between pin-6 and pin-7) so that free running frequency as per equation 9.1 is given by,

$$f_0 = \frac{(0.16).(2.5V)}{(10k\Omega).(0.002\mu F)} + \frac{1}{(100k\Omega).(0.002\mu F)} = 20kHz + 5kHz = 25kHz \quad (9.2)$$

The FM output is obtaned from VCO_{out} (pin-4) of first PLL IC.

Demodulation Use the same R_1, R_2 and C for the second PLL IC so that the free running frequency remains the same as that of the modulating IC. Feed the signal input pin of phase detector (pin-14) of the second IC with the FM signal. The other input of phase detector (pin-3) is fed with VCO output (pin-4).
The output from phase detector(pin-2) is fed back to VCO input (pin-9) through a low-pass filter with $R_3 = 10\ k\Omega$ and $C_1 = 0.01\ 0.01\mu F$.
The demodulated output is obtained from the pin-10 by pulling down using a resistor $R_p = 10\ k\Omega$. It is then low pass filtered at $fc = 1.5kHz$ to eliminate higher order ripples.

$$f_c = \frac{1}{2\pi R_f C_f} = 1.5kHz \quad (9.3)$$

Choose $C_f = 0.01\ \mu F$. $\therefore\ R_f = 10\ k\Omega$.

Circuit Diagram

The circuit diagram for FM modulation and demodulation are shown in figure 9.1.

Procedure

- Make connections as per the circuit digram.
- Provide dc supply and ground to the ICs.
- Observe the FM modulation and demodulation waveforms.
- Plot it on a graph sheet.

Observation

Plot the message, carrier, modulated and demodulated waves on a graph sheet. See Figure 9.2.

Result

Implemented FM modulation and demodulation using PLL IC CD 4046.

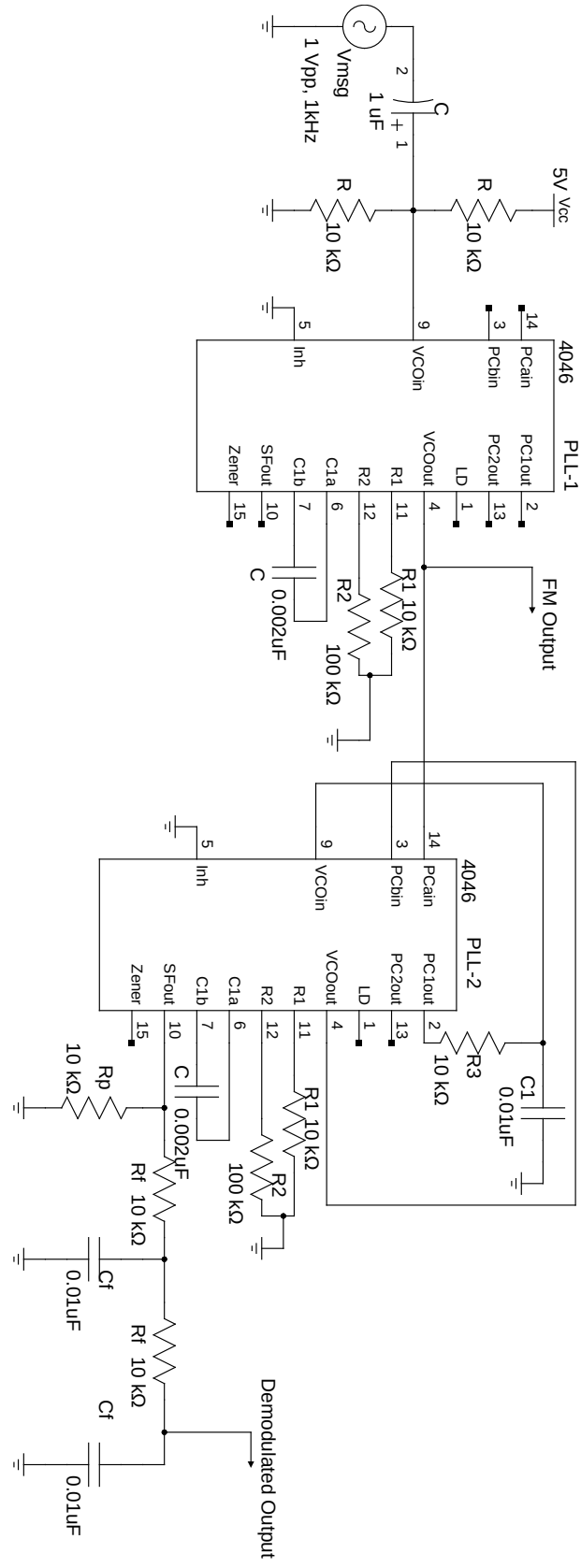

Figure 9.1: Circuit for FM generation and detection using CD4046 PLL IC

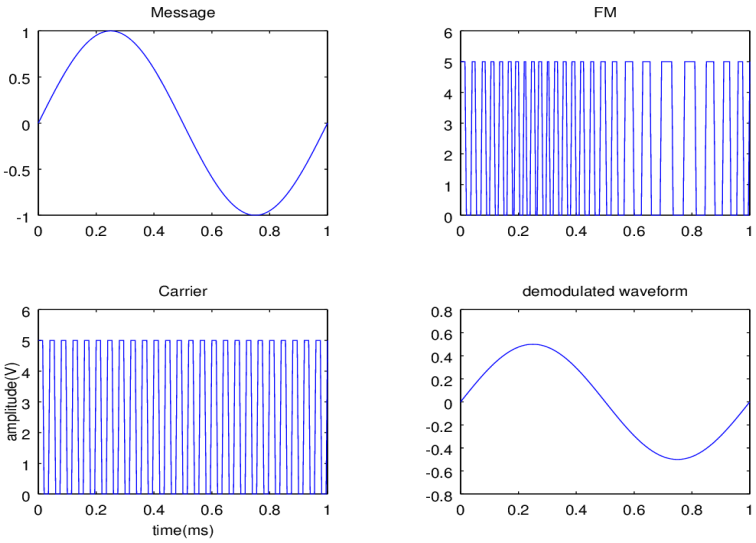

Figure 9.2: FM generation and detection waveforms

Chapter 10

Mixer (Frequency Converter) Circuit using BJT

Aim

To design and set up a frequency converter circuit to produce an output frequency (f_0) which is the difference frequency between the two input frequency, ($f_1 - f_2$).

Theory

A mixer or frequency mixer is a nonlinear electrical circuit that creates new frequencies from two signals applied to it. In its most common application, two signals at frequencies f_1 and f_2 are applied to a mixer, and it produces new signals at the sum $f_1 + f_2$ and difference $f_1 - f_2$ of the original frequencies. Other frequency components (like $f_1 \pm 2f_2$ may also be produced in a practical frequency mixer.[1]

The most important application of mixers are in superhetrodyne receivers where the very high carrier frequency is down converted to an intermediate frequency. This is done by mixing the carrier frequency with a locally generated oscillator frequency to get an output frequency which is the difference between local oscillator frequency and incoming signal frequency, ie the intermediate frequency. In widely used AM receivers the local oscillator frequency is so chosen with respect to carrier frequency such that their difference is a constsnt intermediate frequency of 455kHz.

[1] http://en.wikipedia.org/wiki/Frequency_mixer

$$f_{IF} = f_{oscillator} - f_{carrier} = 455kHz$$

The mixer output which contains all image frequencies of $f_1 \pm nf_2$ is filtered to obtain the required difference frequency $f_1 - f_2$.

Design

Let the input at the base be 10kHz(f_1) signal and at the emitter be 9 kHz(f_2) signal such that the output contains their sum and difference frequencies. The output can be low pass filtered to obtain the difference frequency $f_1 - f_2 = 1\ KHz$.
Choose Transistor BC107. See A.3 for its datasheet details. Take $V_{CC} = 12V$ and $I_C = 2mA$ under dc biasing conditions.
For Class A mode of operation, let

$$V_{CE} = \ 50\%\ of V_{CC} = \ 6V \tag{10.1}$$

$$V_{RC} = \ 40\%\ of V_{CC} = \ 4.8V \tag{10.2}$$

$$V_{RE} = \ 10\%\ of V_{CC} = \ 1.2V \tag{10.3}$$

Design of Emitter and Collector Resistors

$$R_C = \ \frac{V_{RC}}{I_C} = \ \frac{4.8V}{2mA} = \ 2.4k\Omega. \approx 2.2k\Omega(\ standard\ resistor\ value) \tag{10.4}$$

$$R_E = \ \frac{V_{RE}}{I_E} = \ \frac{1.2V}{2mA} = \ 600\Omega. \approx 560\Omega(\ standard\ resistor\ value) \tag{10.5}$$

(Since $I_C \approx I_E = 2mA$)

Design of Potential divider resistors R_1 and R_2
At dc bias point,

$$I_B = \ \frac{I_C}{h_{fEmin}} = \ \frac{2mA}{110} \approx 20\mu A \tag{10.6}$$

Let the current through R_1 be $10I_B$ and that through R_2 be $9I_B$ such that I_B flows through the base of BC107.

$$I_{R1} = \ 10I_B = \ 200\mu A \tag{10.7}$$

$$I_{R2} = \ 9I_B = \ 180\mu A \tag{10.8}$$

Voltage across resistor R_2 is,

$$V_{R2} = V_{RE} + V_{BEactive} = \ 1.2V + 0.6V = \ 1.8V \tag{10.9}$$

$$R_2 = \ \frac{V_{R2}}{I_2} = \ \frac{1.8V}{180\mu A} = \ 100k\Omega \tag{10.10}$$

Voltage across resistor R_1 is,

$$V_{R1} = V_{CC} + V_{R2} = \ 12V - 1.8V = \ 10.2V \tag{10.11}$$

$$R_1 = \ \frac{V_{R1}}{I_1} = \ \frac{10.2V}{200\mu A} = \ 51k\Omega \approx 47k\Omega(\ standard\ resistor\ value) \tag{10.12}$$

Design of coupling capaciors

$C_1 = 1\mu F$ and $C_E = 0.1\mu F$

Design of Filter Circuit

Inorder to lowpass filter the output signal choose the upper cut-off frequency be f_o=1.5kHz so that the required output 1 kHz appears in the pass band. The cut-off frequency of lowpass filter is,

$$f_o = \ \frac{1}{2\pi R_f C_f} = 1.5\ kHz \tag{10.13}$$

where R_f and C_f are the passive filter components.

Choose $R_f = \ 10k\Omega$

$$\therefore C_f = \frac{1}{2\pi R_f f_o} \approx 0.01\mu F. \tag{10.14}$$

Choose π filter configuration for better performance.

Circuit Diagram

See Figure 10.1 for circuit diagram.

Procedure

1. Make connections as per the circuit diagram.
2. Feed f_1 and f_2 with amplitudes as shown in the circuit diagram and frequencies 10 kHz and 9 kHz respectively.
3. Observe the filtered output frequency on a CRO.
4. Repeat with frequencies changed to 20 kHz and 19kHz (50 kHz and 49 kHz)and observe it in CRO. Verify that the circuit gives the difference frequency of 1 kHz at the output.
5. Plot the input and output signals on a graph sheet.

Observation

From the graph find the frequency of the output signal.

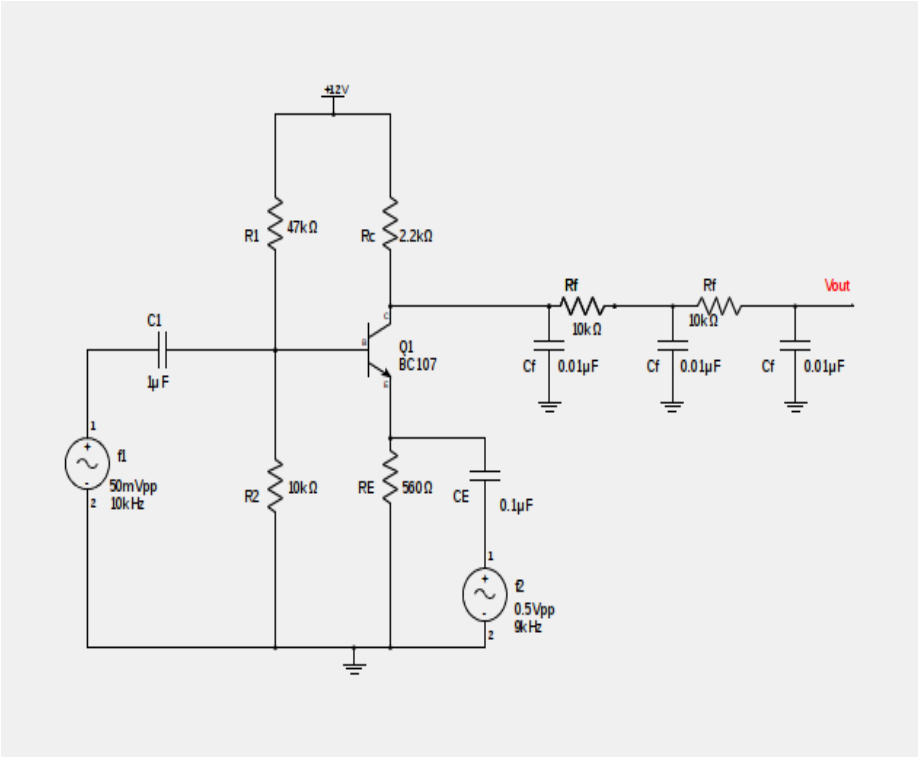

Figure 10.1: Circuit Diagram for Mixer circuit using BJT

Result

The mixer circuit using BJT was set up and output was verified from signals observed on a CRO.

Appendix A

Quick Reference: Component Details

A.1 Intermediate Frequency Transformer

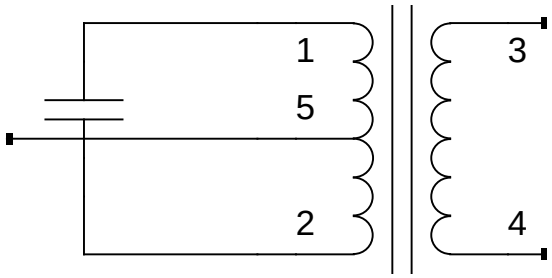

Figure A.1: Schematic diagram of intermediate frequency transformer

Intermediate Frequency Transformers come as specially designed tuned circuits in groundable metal packages called IF cans. The primary winding has an inducance of $L_{eq} = 450\mu H$ and it comes with a shunt capacitor of capacitance $C = 270\ pF$. Its resonant frequency is thus $f = \frac{1}{2\pi\sqrt{L_{eq}C}} \approx 455kHz$.

This frequecy is adjustable by a factor of $\pm 10\%$. IFT has a tapped primary winding as shown in the schematic diagram, Figure A.1.

The ferrite core between primary and secondary windings is tunable with a non-metallic screw driver or tuning tool. It changes the mutual inductance and thus control the Q-factor of the collector circuit of connected transistor[3]. Its internal details are shown in Figure A.2 and physical consruction is shown in Figure A.3 [4]. [1]

[1] Images are taken from: http://retro.co.za/archive/amateur/SM0VPO-ReusingIFCans.pdf

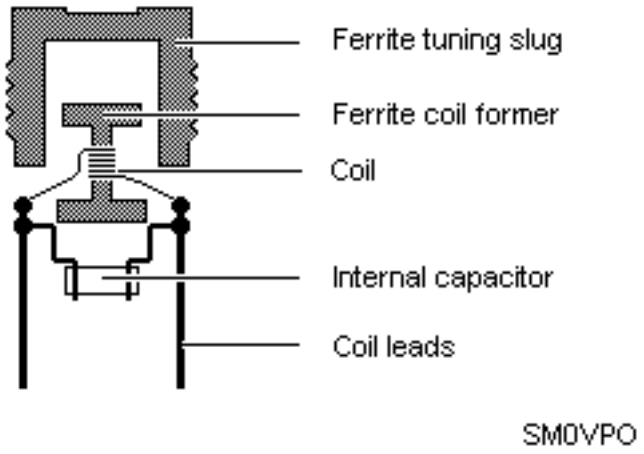

Figure A.2: Internal details of IF CAN

A.2 BJT BF194/195

BF194/195 is a high frequency transistor with the following characteristics.

Type Designator: BF194/BF195
Material of transistor: Si
Polarity: NPN
Maximum collector power dissipation (Pc), W: 0.25
Maximum collector-base voltage $|V_{cb}|$, V: 30
Maximum collector-emitter voltage $|V_{ce}|$, V: 20
Maximum emitter-base voltage $|V_{eb}|$, V: 5
Maximum collector current $|I_{cmax}|$, mA: 30
Forward current transfer ratio (hFE), min: 67

A.3 BJT BC107

Type Designator: BC107
Material of transistor: Si
Polarity: NPN
Maximum collector power dissipation (P_c), W: 0.3
Maximum collector-base voltage $|V_{cb}|$, V: 50
Maximum collector-emitter voltage $|V_{ce}|$, V: 45
Maximum emitter-base voltage $|V_{eb}|$, V: 6
Maximum collector current $|I_{cmax}|$, A: 0.1
Forward current transfer ratio (h_{FE}), min: 110
Package of BC107 transistor: TO18

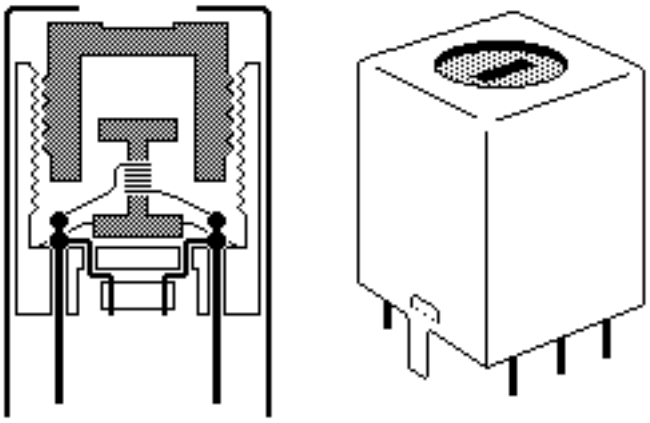

Figure A.3: Physical construction of IF CAN

A.4 CD 4016 - CMOS switching IC

The 4016 contains 4 analogue bilateral switches, each with an active-high enable input (A) and two input/outputs (X and Y). When the enable input is asseted (high), the X and Y terminals are connected by a low impedance; this is the on condition. When the enable is low, there is a high impedance path between X and Y, and the switch is off.

The pinout diagram of 4016 switching IC is shown in Figure. A.4[2].

A.5 AD 633 - Multiplier IC

Multiplier ICs: Analog multipliers are complex arrangements of Opamps and other circuit elements in the form of IC. It can be used for different applications like multiplication, division, squarer, modulator, demodulator, filter etc. There are two inputs **X** and **Y** to which the signals to be multiplied are given. There are two input terminals **X** and **Y** to which the signals to be multiplied are given. The output W is the product of instantaneous values of input signals reduced by a scale factor **k**. **k** is usually less than 1. For practical ICs $\mathbf{k} = \frac{1}{10}$.

$$W = kXY \tag{A.1}$$

AD633 is functionally a complete four quadrant analog multilier IC. The functional block diagram is shown in Fig. A.5. This IC uses Gilbert's transconducatnce multiplier module in four quadrants. On chip circuit provides a scale

[2]Image courtesy:Inductiveload (Own work) [Public domain]via Wikimedia Commons

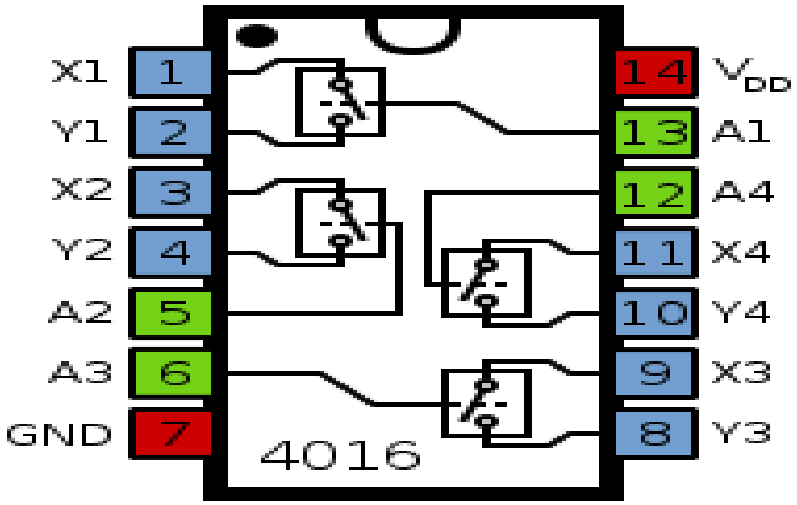

Figure A.4: Pinout Diagram of 4016 switching IC

factor of $k = \frac{1}{10}$. If **X**, **Y** and **Z** inputs are given we get

$$W = \frac{XY}{10} + Z \tag{A.2}$$

Here **Z** is the input to the summing amplifier. If the summing amplifier input is grounded, then output

$$W = \frac{XY}{10} \tag{A.3}$$

Specifications as in AD633 data sheet is,
Dual power supply: $V_{cc} = \pm\ 8V to \pm\ 18V$
Input impedance $> 5M\Omega$
Output impedance $< 75\Omega$
Maximum operating frequency (Bandwidth) $= 1M\Omega$

A.6 555 Timer IC

The 555 timer IC is an integrated circuit (chip) used in a variety of timer, pulse generation, and oscillator applications. The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element. All these circuit variats are achieved by connecting proper values of resistors and capacitors externally. The pinout[3]. of 555 timer IC are shown below.

[3]Image courtesy:Inductiveload (Own work) [Public domain]via Wikimedia Commons

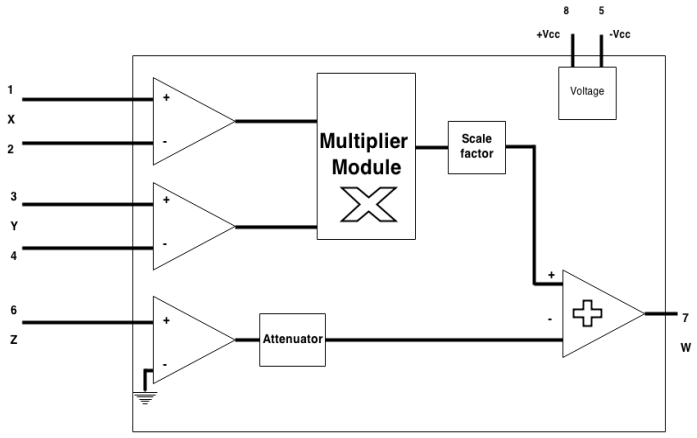

Figure A.5: Functional Block Diagram for AD633 multiplier IC

The functions of various pins of 555 are shown in Table A.1. [4]

Please refer to 555 Timer IC for more detailed working of the IC pins when it is configured as multivibrators or oscillators.

A.7 CD 4046 - PLL IC

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal from an oscillator which is synchronized in phase and frequency with its input signal. It is an electronic circuit consisting of a voltage controlled variable frequency oscillator(VCO), a phase detector and a lowpass filter. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal. Proportional to the phase difference a voltage waveform is generated. It is lowpass filtered to obtain a dc volatge which is proportional to the phase difference. This voltage is fed back to the VCO to control and adjust the oscillator to keep the phases matched. For more details refer [5]. Specifically PLL synchronizes its VCO phase and frequency with the input for a given range of frequencies. The block diagramatic representation of a PLL is shown in Figure. A.7.

The range of input frequencies($f_i = f_{min}$ to $f_i = f_{max}$) for which the the PLL remains in this locked condition is called lock range of the PLL. If PLL is initially locked and the input fequency f_i becomes less than f_{min} or if f_i exceeds f_{max}, PLL becomes unlocked.

When PLL is unlocked, VCO oscillates at free running frequency or centre

[4] https://en.wikipedia.org/wiki/555_timer_IC#Pins

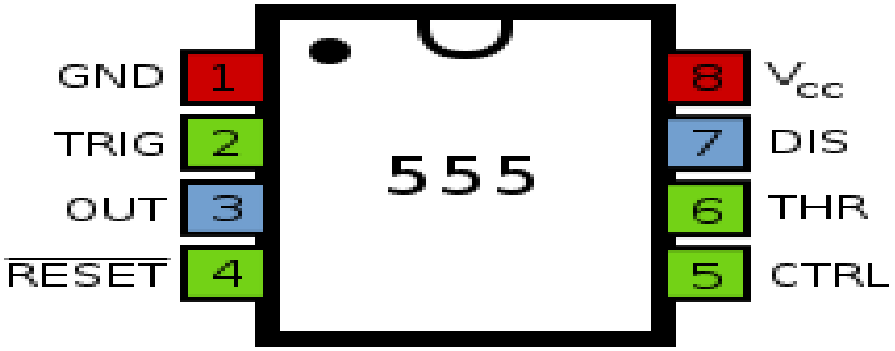

Figure A.6: Pin-out diagram of 555 IC

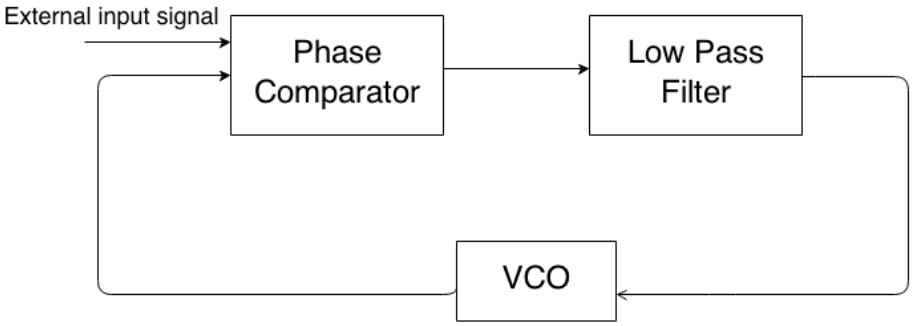

Figure A.7: Block diagram of a PLL

frequency, f_0. The lock can be re-established if f_i becomes sufficiently close to f_0. The range of frequencies around f_0(ie, $f_0 - f_{cap}$ to $f_0 + f_{cap}$) which when applied as input captures a PLL into lock is called capture range of the PLL.

CD4046 is a PLL IC. It has a linear voltage controlled oscillator(VCO) and two phase comparators(PC_1 and PC_2)-*Any of which can be used for PLL operation.* The periodic signal generated by the VCO is the output signal which is synchronized with the input signal.

The amplitude of VCO output depends on V_{cc} and its free running frequency is determined by V_{cc} as well as the value of externally connected resistors and capacitors R_1, R_2 and C. The pinout diagram is shown in the Figure. A.8.

Table A.1: Pin details of 555 IC

Pin number	Name	Purpose
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 of VCC, when CTRL is open).
3	OUT	This output is driven to approximately 1.7 V below +VCC or GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides THR.
5	CTRL	Provides "control" access to the internal voltage divider (by default, 2/3 VCC).
6	THR	The timing (OUT high) interval ends when the voltage at THR is greater than that at CTRL (2/3 VCC if CTRL is open).
7	DIS	Open collector output which may discharge a capacitor between intervals. In phase with output.
8	VCC	Positive supply voltage, which is usually between 3 and 15 V depending on the variation.

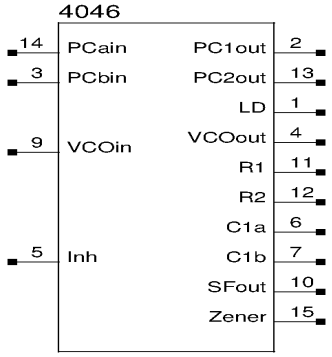

Figure A.8: Pinout diagram of CD4046 PLL IC

Bibliography

[1] LABORATORY MANUAL COMMUNICATIONS LABORATORYEE 321, CALIFORNIA STATE UNIVERSITY, LOS ANGELES Lab-Volt Systems, Inc.

[2] Communication Systems: An introduction to Signals and Noise in Electrical Communication, McGrawHill, Bruce Carlson, Paul Crilly.

[3] Electronic Communication Systems- Fundamentals Through Advanced, Pearson 5ed, Wayne Tomasi.

[4] REUSING TRANSISTOR IF CANS by SM0VPO

[5] Phase Locked Loop, Wikipedia article.